What is claimed is:

1. A non-volatile memory device comprising:

data connections that are compatible with a synchronous dynamic random access memory;

a non-volatile memory array coupled to the data connections;

~~a~~ programmable, volatile register to store protection data;

non-volatile register, coupled to the volatile register, to store default protection data;

a voltage detector to determine if a memory power supply voltage drops below a predetermined level; and

control circuitry to program the protection data and read the volatile and non-volatile registers and prevent erase or write operations to the memory array in response to the read protection data.

2. The memory device of claim 1 wherein the volatile register and the non-volatile register are comprised of multiple bits and are substantially equal in size.

3. The memory device of claim 1 wherein the memory array is arranged in a plurality of addressable blocks and both the non-volatile and volatile register have a plurality of data bits, each of the plurality of data bits is a protection data that corresponds to one of the plurality of addressable blocks.

4. The memory device of claim 3 wherein the memory array has 16 addressable blocks and the programmable register circuitry has 16 corresponding data bits.

5. The memory device of claim 1 wherein the memory array comprises floating gate memory cells.

6. A synchronous non-volatile memory device comprising:

a plurality of data connections that are compatible with a synchronous dynamic random access memory device;

a flash memory array arranged in addressable blocks;

a multiple bit, volatile register to store protection data, where each one of the multiple bits corresponds to one of the addressable blocks of the memory array;

a multiple bit, non-volatile register coupled to the volatile register and acting as a shadow register to store default protection data;

a voltage detector to determine if a memory power supply voltage drops below a predetermined level; and

control circuitry to program the volatile register circuitry and prevent erase or write operations to the memory array in response to the protection data.

7. The memory device of claim 6 wherein the flash memory array is comprised of floating gate memory cells.

8. The memory device of claim 7 wherein the memory array has 16 addressable blocks and the volatile register circuitry has 16 corresponding data bits.

9. The memory device of claim 7 wherein the memory array has 16 addressable blocks and the non-volatile register circuitry has 16 corresponding data bits.

10. The memory device of claim 7 wherein the control circuitry includes a state machine to control erase and write operations.

11. A memory system comprising:

a processor that generates memory device control signals; and

a synchronous non-volatile memory device coupled to the processor and comprising:

a plurality of synchronous dynamic random access memory compatible data connections;

a non-volatile memory array coupled to the data connections;

a programmable volatile register to store protection data;

a non-volatile register, coupled to the volatile register, that stores default protection data;

a voltage detector to determine if a memory power supply voltage drops below a predetermined level; and

control circuitry to program protection data into the volatile register, in response to the memory power supply voltage, and prevent erase or write operations to the memory array in response to the protection data.

12. The memory system of claim 11 wherein the processor is coupled to read data from the volatile register through the data connections.

13. The memory system of claim 12 wherein the status register data indicates a protect status of the memory.

14. The memory system of claim 11 wherein the control circuitry comprises a state machine that performs control functions of the memory device.

15. The memory system of claim 11 wherein the control circuitry loads data from the non-volatile register into the volatile register on power-up.

16. The memory system of claim 11 wherein the control circuitry programs data from the volatile register to the non-volatile register on either a power-down or a reset operation.

17. A method of operating a non-volatile, synchronous memory device having data connections that are compatible with a synchronous dynamic random access memory device, the method comprising:

on power-up, transferring default protection data from a non-volatile register to a volatile register;

monitoring a power supply voltage coupled to the memory device; and

prohibiting write or erase operations from being performed when the supply voltage drops below a predetermined value.

18. The method of claim 17 further comprises setting a content of the non-volatile register to a protection status when the supply voltage drops below a predetermined value.

19. The method of claim 18 wherein the write or erase operations are prohibited based upon the content of the non-volatile register.

20. The method of claim 17 further comprising:

performing a reset operation on the memory device after the supply voltage drops below the predetermined value; and

allowing write or erase operations to be performed after the reset operation is performed.

21. The method of claim 20 further comprises setting a content of the non-volatile register to a protection status when the supply voltage drops below a predetermined value, and setting the content of the non-volatile register to a default status when the reset operation is performed.

22. The method of claim 17 wherein the memory device comprises memory cells arranged in X-addressable blocks, and the method further comprises setting a content of an X-bit register

23. The method of claim 17 and further including transferring the default protection data from the non-volatile register to the volatile register after a reset operation.